PREPARED BY: DATE	SHARP	SPEC No. LA-07A02
		FILE No.
APPROVED BY: DATE		ISSUE Nov. 14. 1995
		PAGE 22
	LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION	APPLICABLE DIVISION
	SPECIFICATION	☐ DUTY DEVELOPMENT CENTER ☐ TFT DEVELOPMENT CENTER ☐ LCD PRODUCTS DEVELOPMENT CENTER ■ EL PRODUCTION DEPT.

SPECIFICATION FOR

EL Display Module

MODEL No. LJ64H051

☐ CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED

BY H. Kishishita

H. Kishishita
Department General Manager
EL Production Department
Naru Factory
Liquid Crystal Display Group
SHARP CORPORATION

SHARP

1. Application

This data sheet is to introduce the specification of EL display module, LJ64H051.

2. Overview

The Sharp EL display module consists of a thin film EL panel, high voltage ICs for panel driving and a display control circuit. By supplying eleven input signals of CMOS level and two DC power supplies of +5 V and +12 V arbitrary graphs and characters can be displayed.

3. Mechanical Specifications

Parameter	Specification Width x Height x Depth	Module
Outline dimensions	246 x 206 x 23.5 (Note 1)	mm
Number of matrix electrodes	640 x 480	--
Active area	191.9 x 143.9	mm
Dot pitch	0.30 x 0.30	mm
Dot pitch ratio	1 x 1	mm
Dot size	0.220 x 0.205	mm
Mass	800	g

Note 1) Details of outline dimensions are shown at Page 13.

4. Absolute Maximum Ratings

4 - 1 Electrical absolute maximum ratings

(Ta=25 ℃)

Parameter	Symbol	Rating	Module
Interface signal (Logic "H")	V_{IH}	V_L+0.3	V
Interface signal (Logic "L")	V_{IL}	-0.3	V
Supply voltage (Logic)	V_L	+7	V
Supply voltage (panel drive)	V_D	+14	V

SHARP

5. Electrical Characteristics

(Ta=25 ℃, Frame frequency=120 Hz)

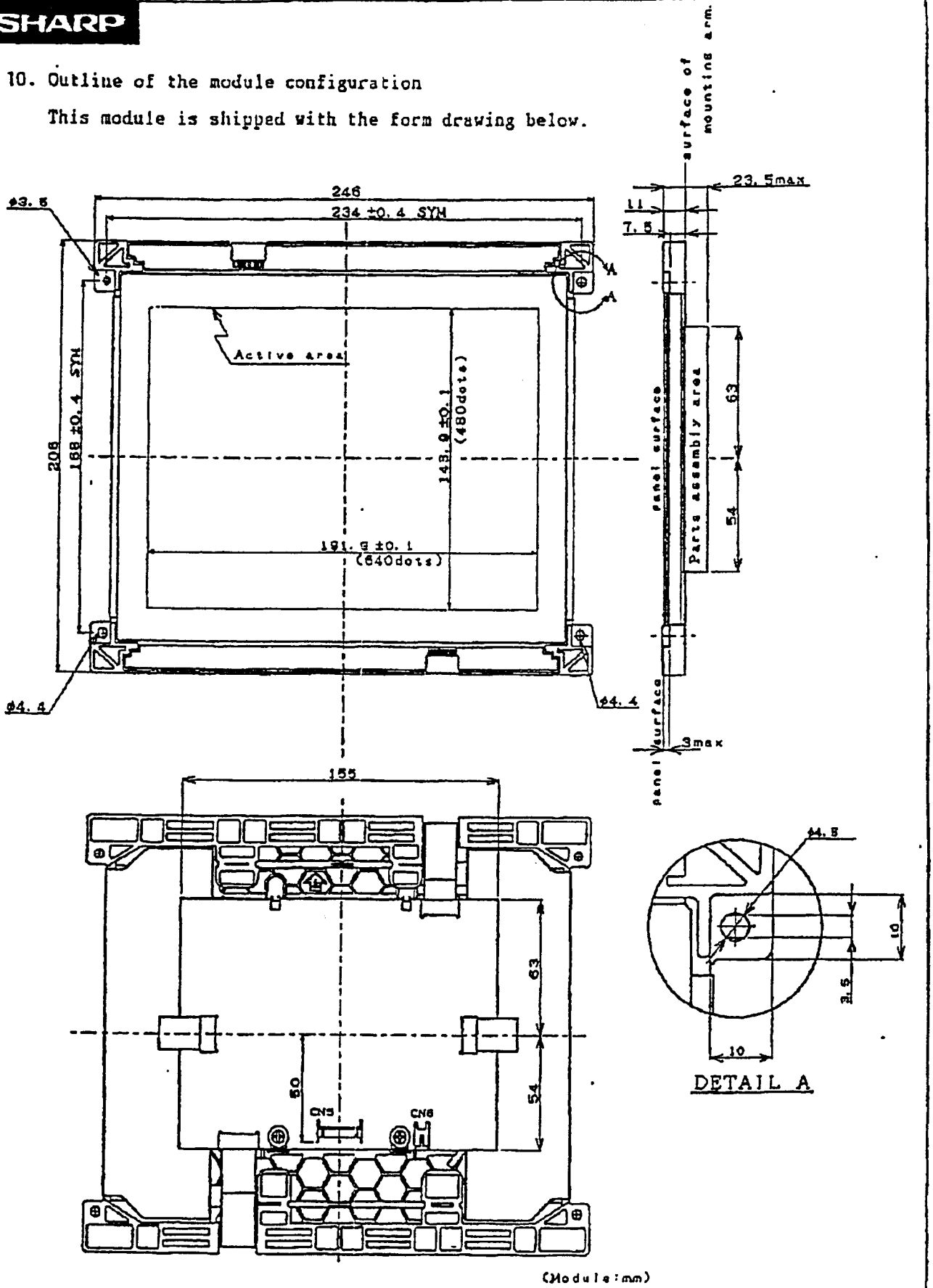
Parameter	Symbol	Rating			Module
		Min.	Typ.	Max.	
Supply voltage (Logic)	V_L	+ 4.75	+ 5.0	+ 5.25	V
Supply current (Logic, V_L=+5 V)	I_L	30	—	300	mA
Supply voltage (Panel drive)	V_D	+ 11.4	+12.0	+12.6	V
Supply current (Panel drive, V_D=+12 V)	I_D	(※1)	—	1500	mA
Total power (V_L=+5 V, V_D=+12 V)	P_T	—	11	—	W

(※1) 10 mA in condition with no signals nor V_L supplying.

SHARP

10. Outline of the module configuration

This module is shipped with the form drawing below.



(Module:mm)

Note) Unspecified tolerance to be ±0.5

SHARP

6. Opical Characteristics

(Ta=25 ℃, Frame frequency=120 Hz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Module	Remark
Luminance	L_{ON}	All dots lit	137	200	—	cd/m²	Note 1)
OFF luminance	L_{OFF}	All dots turned off	—	—	3.4	cd/m²	
Luminance distribution	ΔL_{DIS}	All dots lit	—	—	35	%	
Fill factor			—	0.50	—		Note 2)
Shadowing characteristics	ΔL_{SD}	fixed pattern	—	2	—	%	Note 3)
Viewing angle			—	160	—	°	

Note 1) Average luminance measured at the dots in circular windows (R1~R5) shown in Fig.1 (Circular window diameter: ϕ 13 mm)

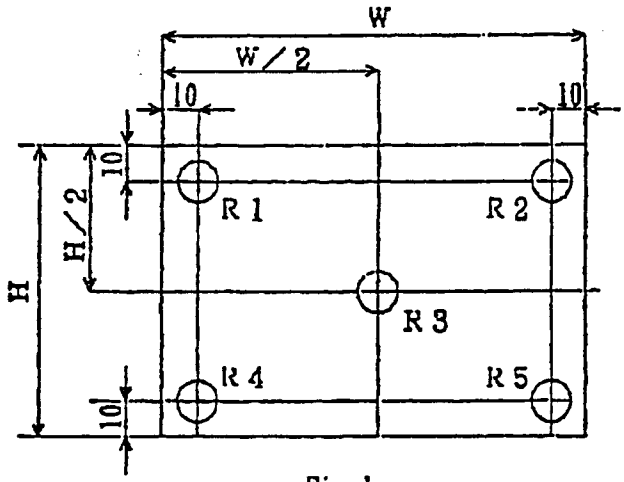


Fig.1

H 143.9 : Height of active area

W 191.9 : Width of active area

Module : mm

Tolerance of luminance: ±10 %

The following formula defines the luminance distribution:

$$\Delta L_{DIS} = (1 - \frac{L_{MIN}}{L_{MAX}}) \times 100 \ (\%)$$

where L_{MAX} is the maximum luminance and L_{MIN} is the minimum luminance taken at the five locations in Fig.1.

SHARP

7. Timing Characteristics

7-1 Input signals

This module is driven by line-at-a-time scanning method with following 11 CMOS level input signals.

Parameter	Symbol	Description	
Data input clock signal	CP2	Clock signal for inputting the display data into the EL unit.	
Display data signal	UD0-3	Data signal for the upper part of display	The signals are sampled at every falling edge of the data input clock signal. The display is "ON" while the logic is "H" and "OFF" while the logic is "L".
	LD0-3	Data signal for the lower part of display	
Input data latch signal	CP1	This signal controls the "timing of line at-a-time scanning" and the "latch timing of the data side shift register on falling edge."	
Scan start-up signal	S	This signal controls frame frequency. And the contents of the display data signal are displayed on the first line by combination with this signal.	

SHARP

7 – 2 Input signals timing characteristics

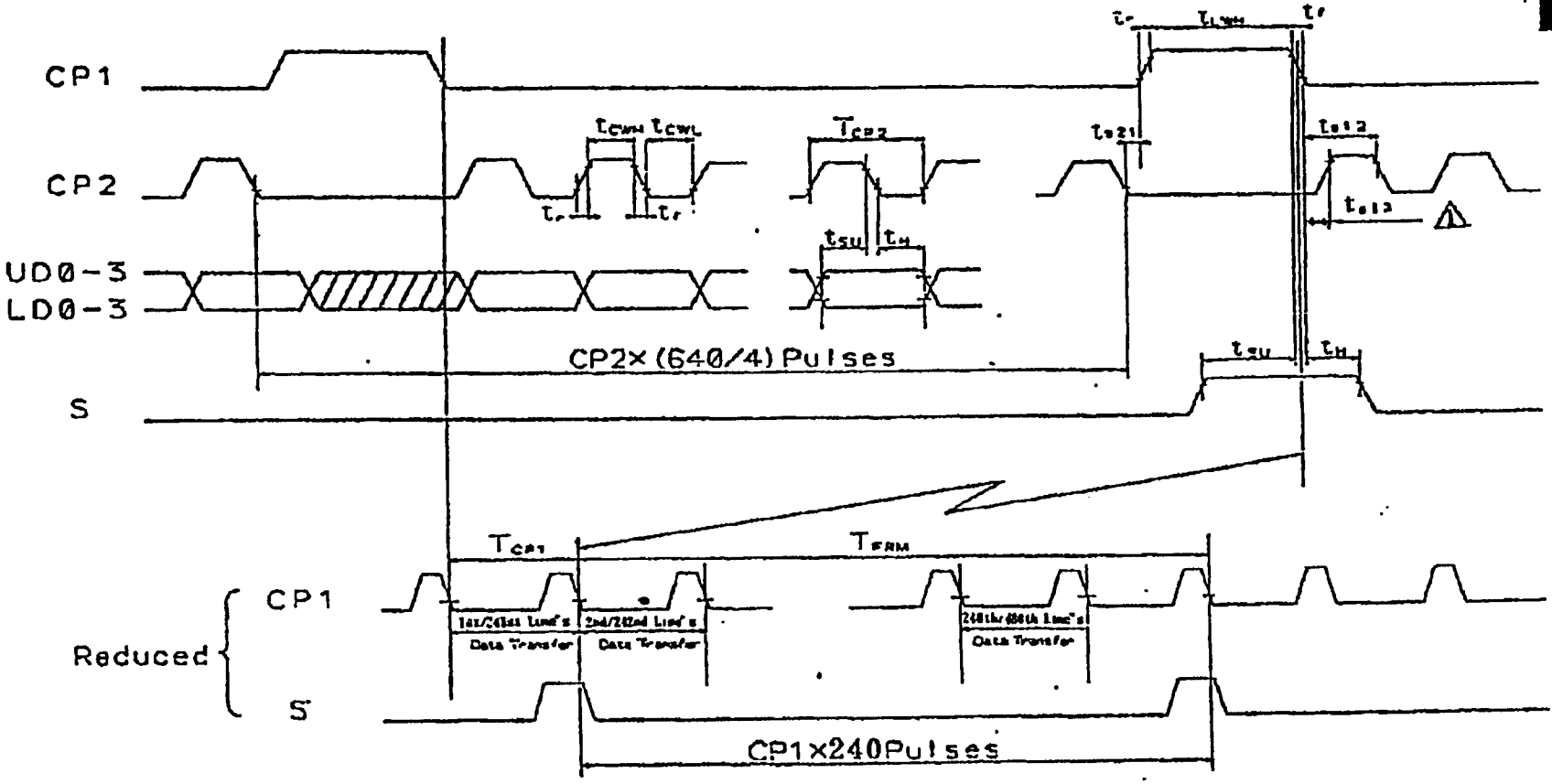
(Ta = 25 ℃)

Parameter	Symbol	Min.	Typ.	Max.	Module
Frame frequency	$1/T_{FRM}$	60	–	120	Hz
CP2 clock cycle	T_{CP2}	154	–	–	n s
High level clock width	t_{CWH}	60	–	–	n s
Low level clock width	t_{CWL}	60	–	–	n s
CP1 clock cycle	t_{CP1}	31	–	–	μ s
High level latch clock width	t_{LWH}	60	–	–	n s
Data set up time	t_{SD}	50	–	–	n s
Data hold time	t_H	40	–	–	n s
CP1↓ clock allowance time from CP2↓	t_{SS1}	0	–	–	n s
CP2↓ clock allowance time from CP1↓	t_{S12}	200	–	–	n s
CP2↓ clock allowance time from CP1↑	t_{S10}	100	–	–	n s
Clock rise/fall time	t_r, t_f	–	–	t_{rf} *	n s

* $t_{rf} = (T_{CP2} - t_{CWH} - t_{CWL}) / 2 \leq 30$ n s max

Note) The vertical blanking time ($T_{FRM} - T_{CP1} \times 240$) shall be minimized to avoid the flickering lines around the center of the display. (around 240th and 241st horizontal lines)

7－3 Input signals timing chart.



V_{IH} = 3.5 V(Min.)
V_{IL} = 1.5 V(Max.)

Note 1) CP1×240 pulses shall be kept.

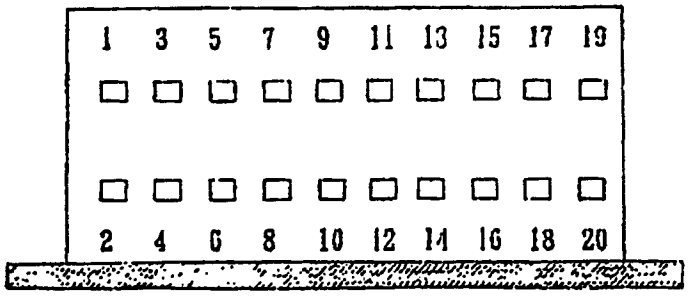
SHARP

8 – 1. Interface signals and power supply connectors

Assignment of pins of connector CN5

No.	SIGNAL	No.	SIGNAL
1	UD1	2	UD0
3	UD3	4	UD2
5	LD1	6	LD0
7	LD3	8	LD2
9	CP2	10	GND
11	CP1	12	GND
13	S	14	GND
15	GND	16	GND
17	+ 5 V	18	+ 5 V
19	+12 V	20	+12 V

Arrangement of pins of connector CN5



Connectors

	Model No.	Maker
Module-side pin header	DF11-20DP-2DS or equivalents	HIROSE ELECTRIC CO.
Fitting socket (crimp contact)	DF11-20DS-2C or equivalents (DF11-2428SC)	HIROSE ELECTRIC CO.

Note 1) The length of the cable shall not exceed 50 cm.

Note 2) This module is not supplied with the fitting socket and the cable.